FORM PTO-1390 (REV. 1-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

# TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

| ATTORNEY'S DOCKET NUMBER | U.S. APPLICATION NO. (If known, see 37 CFR 1.5) |
|---|---|
| 3672-0109P | 09/720084 NEW |

| INTERNATIONAL APPLICATION NO. | INTERNATIONAL FILING DATE | PRIORITY DATE CLAIMED |
|---|---|---|
| PCT/NO00/00137 | April 27, 2000 | April 30, 1999 |

**TITLE OF INVENTION**
AN APPARATUS COMPRISING ELECTRONIC AND/OR OPTOELECTRONIC CIRCUITRY AND METHOD FOR *

**APPLICANT(S) FOR DO/EO/US**
EBBESEN, Thomas; NORDAL, Per-Erik

**Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:**

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau). WO 00/67539
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(3)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

**Items 11. to 16. below concern document(s) or information included:**

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.-1449 and International Search Report (PCT/ISA/210) w/ 5 documents

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    1.) PCT Request(PCT/RO/101)
    2.) Thirteen (13) sheets of Formal Drawings



*REALIZING SAID CIRCUITRY

| U.S. APPLICATION NO (if known, see 37 CFR 1.5) | INTERNATIONAL APPLICATION NO | ATTORNEY'S DOCKET NUMBER |
|---|---|---|
| 09/720084 NEW | PCT/NO00/00137 | 3672-0109P |

17. ☒ The following fees are submitted:

| | | CALCULATIONS | PTO USE ONLY |
|---|---|---|---|
| **BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):** | | | |
| Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO | **$1,000.00** | | |
| International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO | **$860.00** | | |
| International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO | **$710.00** | | |
| International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) | **$690.00** | | |
| International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) | **$100.00** | | |
| **ENTER APPROPRIATE BASIC FEE AMOUNT =** | | **$ 1000.00** | |
| Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)). | | **$ 0** | |

| CLAIMS | NUMBER FILED | NUMBER EXTRA | RATE | | |
|---|---|---|---|---|---|
| Total Claims | 34 - 20 = | 14 | X **$18.00** | **$ 252.00** | |
| Independent Claims | 2 - 3 = | 0 | X **$80.00** | **$ 0** | |
| MULTIPLE DEPENDENT CLAIM(S) (if applicable) | | None | + **$270.00** | **$ 0** | |
| | | **TOTAL OF ABOVE CALCULATIONS =** | | **$ 1252.00** | |
| Reduction of ½ for filing by small entity. **Applicant claims small entity status (See 37 C.F.R. § 1.27)** | | | | **$ 0** | |
| | | **SUBTOTAL =** | | **$ 1252.00** | |
| Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). | | | + | **$ 0** | |
| | | **TOTAL NATIONAL FEE =** | | **$ 1252.00** | |
| Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property | | | + | **$ 40.00** | |
| | | **TOTAL FEES ENCLOSED =** | | **$ 1292.00** | |
| | | | | **Amount to be: refunded** | **$** |
| | | | | **charged** | **$** |

a. ☒ A check in the amount of $ **1292.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448.

**NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.**

Send all correspondence to:
**Birch, Stewart, Kolasch & Birch, LLP or Customer No. 2292**
**P.O. Box 747**
**Falls Church, VA 22040-0747**
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SIGNATURE

MUTTER, MICHAEL K.
NAME

#29,680 (MKM)
REGISTRATION NO.

/c ember 20, 2000

(REV. 09/29/2000)

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: EBBESEN, Thomas et al.

Int'l. Appl. No.: PCT/NO00/00137

Appl. No.: New Group:

Filed: December 20, 2000 Examiner:

For: AN APPARATUS COMPRISING ELECTRONIC AND/OR OPTOELECTRONIC CIRCUITRY AND METHOD FOR REALIZING SAID CIRCUITRY

PRELIMINARY AMENDMENT

**BOX PATENT APPLICATION**
Assistant Commissioner for Patents
Washington, DC 20231

December 20, 2000

Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

**AMENDMENTS**

**IN THE SPECIFICATION:**

Please amend the specification as follows:

Before line 1, insert --This application is the national phase under 35 U.S.C. § 371 of PCT International Application No. PCT/NO00/00137 which has an International filing date of April 27, 2000, which designated the United States of America.--

**IN THE DRAWINGS:**

Please substitute the attached new Figure 7 for the original Figure 7 filed with the international application.

**REMARKS**

The specification has been amended to provide a cross-reference to the previously filed International Application. The claims have also been amended to delete multiple dependents and to place the application into better form for examination. Entry of the present amendment and favorable action on the above-identified application are respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Michael K. Mutter, #29,680

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MKM/cqc
3672-0109P

(Rev. 04/19/2000)

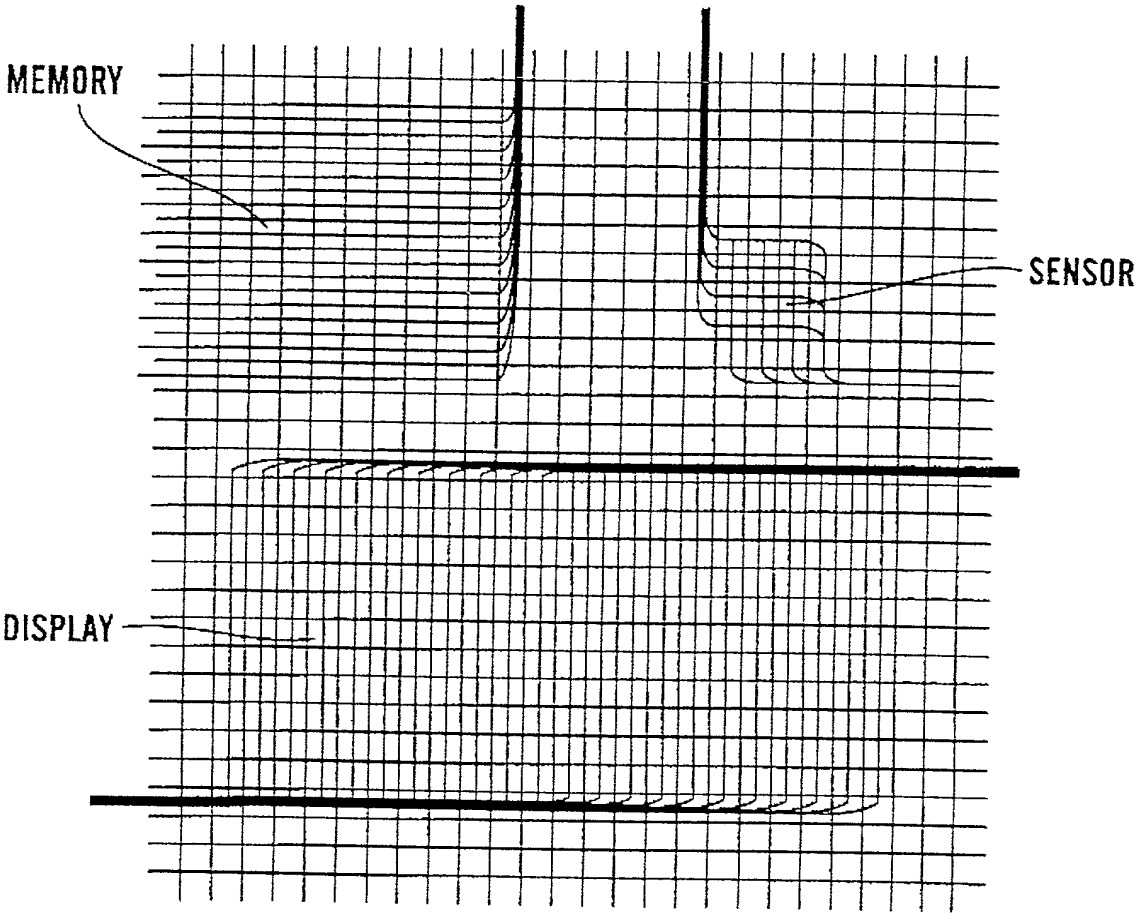


Fig.7

# An apparatus comprising electronic and/or optoelectronic circuitry and method for realizing said circuitry

The present invention concerns an apparatus comprising electronic and/or optoelectronic circuitry for implementing electronic and/or optical functions, wherein the circuitry is realized and/or integrated in two or more dimensions and a method for method for realizing and/or integrating circuitry in two- or more dimensions, wherein the circuitry comprises elements in the form of wires, fibres, ribbons, strips or multicomponent filaments and/or combinations thereof, wherein said circuitry is electronic and/or optoelectronic circuitry for implementing electronic and/or optical functions in an apparatus comprising circuitry of this kind.

In particular, the present invention concerns integrating filament-like electrical and/or optical conduits into two- and three-dimensional physical structures for creating electronic or optoelectronic circuitry, sensors and/or emitters. The spatial extent or region of influence of such circuitry, sensors and/or emitters is controlled by specific definition of the electrical and/or optical properties of the individual filaments and how they are incorporated into the structures.

The development of integrated circuits on silicon and semiconductor compound materials has revolutionized the electronic industry. However, the ever increasing complexity and costs of higher integration technology has generated interest in novel materials and methods.

For instance, progress in conductive polymers and organic materials has led to novel displays, diodes and field-effect transistors using these materials. See G. Horowitz "Organic field effect transistors" Adv. Mat. Vol. 10, pp. 365-377 (1998); D. Pede & al. "A general-purpose conjugated-polymer device array for imaging" Adv. Mat. Vol 10, pp. 233-237 (1998); R.H.Friend et al. "Electroluminescence in Conjugated 'Polymers", Nature 397, pp.121-128 (1999).

Thin-film-based inorganic semiconductor technologies compatible with low temperature-resistant packaging and substrate materials are under rapid development, and include amorphous silicon as well as polysilicon and microcrystalline silicon. In this connection, see, e.g. J.G. Blake & al.,

"Low-temperature polysilicon reshapes FPD production", Solid State Technology, pp.151-161 (May 1997).

Defect tolerant architectures have been proposed to circumvent the problems of trying to produce defect free chips, for instance by J.R. Heath & al., "A defect-tolerant computer architecture: opportunities for nanotechnology", Science, Vol. 280, pp. 1716-1721 (June 12, 1998).

Such novel materials and methods open up entirely new opportunities in electronics and optoelectronics that extend much beyond providing an evolutionary route to alleviating problems and limitations adhering to the present state of the art. Unfortunately, present-day semiconductor-oriented technologies are totally inadequate for exploiting the true potential of these novel materials and methods, and there exist pressing needs for complementing technologies. One area of particular importance is that of gaining freedom from the dominating role of the substrate.

In traditional silicon-based technologies, the electronic functionality is derived from the semiconducting silicon substrate, which severely restricts opportunities for extensions into the third dimension. Furthermore, physical dimensions are restricted, and the traditional lithographic processes provide only limited flexibility with respect to intra-device connectivity. This includes both the physical characteristics of the connecting lines themselves and how they can be positioned throughout the device structures in question. Typically, the substrate and its layered superstructures contain electrical interconnects where electric currents flow in patterned strip- or ribbon-like conducting paths that have been created by subtractive or additive processes.

Subtractive processes are well-known and much used in the semiconductor industry, and involve wet or dry etching whereby conducting material is removed from portions of the substrate. Conducting material is retained in regions where a protective layer has been applied in the patterns desired, e.g. by optical lithography. Typically, all modern microelectronic circuits involve multiple step lithography processes where image(s) of parts or all of the circuitry, mostly wires, and devices are transferred to the substrate. This requires careful register between each step, the more so as the features become smaller and smaller. The substrate must be extremely flat and rigid. Furthermore, the circuitry cannot be continuous through this approach. Several chips have to be made individually on one wafer at the time.

Furthermore, the integration of electronic and optoelectronic circuits is extremely difficult by such methods. It would therefore be highly advantageous to find microcircuit fabrication methods which eliminate lithographic processes altogether and allow for flexible continuous fabrication of electronic and optoelectronic circuits.

Additive processes have hitherto been less used in electronic circuits, but may become important in the future. They include microprinting and micromolding of conducting inks or solid state conductors, screen printing and more exotic means such as laser mediated deposition (see, e.g.. H. Yabe & al., "Direct writing of conductive aluminum line on aluminum nitride ceramics by transversely excited atmospheric CO2 laser", APL 71 2758 (1997)).

The present invention introduces the concept of woven electronics as a new generic approach to making and assembling electronic and optoelectronic devices and apparatus, in particular by exploiting opportunities that arise with the advent of novel electronic materials. This implies a radical departure from present state of the art. Indeed, literature searches have been performed without being able to identify any relevant prior art. For the sake of completeness, however, those patent documents that were retrieved by the search profiles employed shall be listed here:

A) DE 31 16 348 A1. "Elektrische Verbindungseinrichtung"; inventor Oscar Alonso, USA.

B) JP 05299533. "Electronic part mounting board and electronic part device using the same"; inventor Ohigata Naoharu, Japan.

C) WO96/38025 A1. "Composite materials"; inventor George William Morris, Great Britain.

Publications A and C describe substrates which incorporate woven layers with electrical conduits. The latter are, however, applied after the weaving process has been finished, by etching, printing or electron sputtering.

Publication B describes a woven structure incorporating conducting wires interspersed with electrically insulating filaments. However, focus is on providing alternative substrates to replace circuit mounting boards subjected

to thermal and mechanical stress, which does not represent any principally new functionality or apparatus impinging on the present invention.

Conducting metallic wires are known to be incorporated by weaving into a wide range of objects. This includes meshes to act for instance as screens in houses, and electrodes and filters in material science. Metallic fabrics and metallic embroidery are used to make decorative and protective clothes. Conducting wires are also integrated into fabrics to provide clothing and furniture free of electrostatic build-up or alternatively to provide electrical heating. In so-called "smart clothes", electronic devices and sensors are attached to the clothes and apparels. See S.E. Braddock and M. O'Mahony, "Techno Textiles-Revolutionary Fabrics for Fashion and Design", chap. 2, Thames & Hudson, New York 1998. Such applications are outside the scope of the present invention, however.

To conclude, in order to realize the potential in a wide range of emerging electronic and optoelectronic materials and methods, there is a need for complementing technologies which are not within the present-day state of the art. Prominent among such technologies are those that can provide electrical and optical interconnections in two and three dimensions, with high spatial density, high signal speed potential and small crosstalk. Also prominent are technologies and materials suitable as structural platforms for large area electronics and/or three dimensional device architectures.

A primary object of the present invention is to provide a lithography-free process to produce electronic and optoelectronic devices, apparatus and circuits in sheet-like or fabric form, or in three dimensional structures.

It is a further object of this invention to provide for continuous circuits over large areas and in mechanically flexible final products which can be shaped to a desired environment or form factor.

It is still a further object of the present invention to provide intra- and inter-device electrical and optical connections that can carry high-speed signals with very low crosstalk.

Another object of the invention is to provide methods to integrate electronic and optical circuits in a continuous matrix.

Yet another object of the invention is to create functional devices by weaving, knitting, crocheting, knotting, stitching and/or combinations thereof.

The above objects and advantages are according to the invention realized with an apparatus which is characterized in that the circuitry comprises elements in the form of wires, fibres, ribbons, strips, or multicomponent filaments and/or combinations thereof, said elements interfacing in a predetermined pattern such that said circuitry are realized with intersections in physical or near physical contact between the elements thereof, that said predetermined pattern is generated by integrating physically two or more of said elements in a fabric-like structure by any of the following processes, viz. weaving, knitting, crocheting, knotting, stitching and/or combinations thereof, that said elements include transparent, non-transparent, conducting, semiconducting or isolating materials and/or combinations thereof, that at least some of said elements according to their material properties form electrical or optical transmission lines or isolators in said circuitry, said electrical or optical transmission lines conveying respectively electrical or optical energy between points and/or areas in said fabric-like structure, that at least some of said elements comprise spatially defined extended active regions, and that at least some of said elements in portions of said fabric-like structure are adapted for emitting or absorbing electrical, chemical, mechanical or optical energy or by interacting with each other by an exchange of energy of the aforementioned kinds; and a method which is characterized by joining two or more elements into a fabric-like structure by any of the following processes viz. weaving, knitting, crocheting, knotting, stitching and/or combinations thereof, such that the elements interfaces in a predetermined pattern, whereby the circuitry is realized with the elements intersecting in physical or near-physical contact in the fabric-like structure, said elements being made of transparent, non-transparent conducting, semiconducting or isolating materials and/or combinations thereof.

In an advantageous embodiment of the apparatus according to the invention, the elements are provided in the predetermined pattern forming a substantially two-dimensional fabric-like structure, while in another advantageous embodiment of the apparatus according to the invention the elements are provided in the predetermined pattern forming a substantially three-dimensional fabric-like structure. In the latter embodiment the elements

then preferably each are provided in a spatial distribution such that the position of the end-points of the elements in the fabric-like structure defines a spatial pattern or grid.

In advantageous embodiments of the apparatus according to the invention it is preferred that some of the transmission lines respectively are twisted pairs, coaxial cables, strip lines or optical fibres.

In the apparatus according to the invention it is advantageous that the active regions of the elements are defined by exposing portions of the said elements to the exterior surroundings thereof. Preferably are then the active regions of an element lengthwise extended therein or an active region of an element corresponds to an end-point thereof.

In the apparatus according to the invention it is advantageous that some of the elements are provided with a protective shielding or cladding, the active regions in these elements being provided by removing the shielding or cladding at selected portions thereof, or alternatively the active regions of the elements are provided in selected portions of the elements exposed in the surface of the fabric-like structure or protruding therefrom at selected locations thereof.

According to the invention are preferably the active regions of the elements defined by exposing portions thereof to spatially selective physical or chemical influences. In the latter case it is then preferred that some of the transmission lines are at least one conductor embedded in an exterior cladding comprising at least one organic semiconducting material, and that active regions are defined therein by contacting said transmission lines with other transmission lines of the same kind or with other transmission lines in intersection which comprises at least one non-isolated or unclad conductor only, whereby semiconducting junctions are formed at the contact points of said intersections . In this case it is preferred that the semiconducting junctions are formed spontaneously upon contacting, or that at least one of the semiconducting junctions are a diode junction, or that the organic semiconducting material is a semiconducting conjugated or non-conjugated polymer.

In the apparatus according to the invention it is advantageous that at least some of the elements over some of their length are shielded against any

interactions in form of an exchange of energy between each other or the exterior surroundings, whereas one or more unshielded portions thereof are adapted for interactions of this kind. and it is then preferred that the unshielded portions of the elements are located at the intersections thereof.

In yet another advantageous embodiment of the apparatus according to the invention it is a two- or three-dimensional optoelectronic display. and the elements are then preferably signal transmission lines. Wherein the display is a two-dimensional display are then the elements provided in a two-dimensional array, preferably such that the elements intersect in a substantially regular pattern or grid, said elements at the intersections thereof being adapted for absorbing or emitting electrical or optical energy. In this case a portion of at least one element in an intersection can be a pixel of the display.

Wherein the display is a three-dimensional display, it is according to the invention preferred that the elements are provided with a predetermined pattern in a three-dimensional array, and then preferably that the elements intersect in a spatially regular pattern or grid, said elements in the intersections thereof being adapted for emitting or absorbing electrical or optical energy. In this case is preferably a portion of at least one element in an intersection a pixel of the display.

Wherein the display is a three-dimensional display with the active regions of the elements provided in selected portions of the element exposed in the surface of the fabric-like structure protruding therefrom at selected locations thereof, it is preferred that the active regions of this kind are pixels in the display, said active regions being either a loop-like portion of an element or an end-point thereof.

Finally it is in the apparatus according to the invention advantageous that it comprises respectively discrete electronic, optoelectronic or optical devices or combinations thereof, and one or more discrete devices can then preferably be physical or chemical sensors connected to at least one of the elements.

In the apparatus according to the invention it can alternatively be advantageous that one or more of the elements are a physical or chemical sensor.

In the method according to the invention it is advantageous providing the surface of the elements with a shielding or cladding material before joining into the fabric-like structure, and removing said shielding or cladding material after the joining into the fabric-like structure from some elements or from selected portions thereof at selected locations in the fabric-like structure.

The invention shall now be described in more detail, with discussions of exemplary non-limiting embodiments showing various embodiments of the present invention and in conjunction with the appended drawings, wherein

figure 1 shows example of basic weaves such as the plain (a), the triaxial (b), the twill (c), the leno (d) and the satin (e) weaves,

figure 2 examples of knits such as the plain (a), the double (b), a warp (tricot) (c) knits and various weft knit stitches (d),

figure 3 examples of multicomponent fabrics such as the weft insertion warp knit fabric (a), pile (b) and carpet (c) fabrics,

figure 4a-e examples of possible shapes and compositions of the fibers, wires and ribbons composing the electronic or optoelectronic fabric,

figure 5 a simple loop detector woven into the fabric matrix,

figure 6 a detector using a pile of fibers as sensor,

figure 7 the integration of various functional units into the fabric matrix,

figure 8a-c a display panel or a two-dimensional photo-detector,

figures 9a,b,c,d principles and embodiments of memory or switching arrays according to prior art and according to the present invention,

figures 10a, 10b and 10c dual-conductor structures of relevance as weaving filaments, and

fig. 11 an example of an apparatus realized as a flexible sheet-like structure.

After a discussion of general aspects of the invention, examples of embodiments shall be given.

As already stated, the given objects of the invention are specifically realized by weaving, knitting, crocheting, knotting and/or stitching a combination of

conducting, semiconducting, superconducting and/or insulating wires or fibers and/or optical fibers. These techniques, in the following also termed joining processes, provide a high degree of control and constructive flexibility in creating integrated physical structures with electrical and/or optical functionality in two and three dimensions.

Control is in part related to the use of strands in the weaving, knitting, crocheting, knotting and/or stitching processes that are pre-made under precisely controllable conditions before being incorporated into the final structure. Each strand can be made to include several different materials and sub-structures, e.g. in the form of electrical multiconductor cables, metallic filaments cladded with polymers that engender electronic functionality when brought into contact with other components in a woven structure, or optical fibers with cladding for protection or environmental sensing.

Control is also a consequence of the degree of topographic order in 2 and 3 dimensions that can be achieved by weaving, knitting, crocheting, knotting and/or stitching processes, where the identity and relative positions of the strands are strictly defined according to a predetermined protocol.

Flexibility in creating 2- and 3-dimensional physical structures and achieving associated electronic and/or optical functionality springs from the diversity and sophistication that can be achieved by weaving, knitting, crocheting, knotting and/or stitching processes, as demonstrated by the present state of the art within the textile industries. With the advent of woven electronics, computer-aided design and manufacturing shall become important tools for creating new architectures and processes specifically targeting the needs and opportunities in that field.

Flexibility is also achieved by the absence of fundamental physical size limits: The strands in the weave may be as long as required for any given application and the ensuing circuit or apparatus may be scaled in size, in principle without limit. The form factor , i.e. size and shape of the woven apparatus may be chosen with few constraints, examples include thin sheets as well as complex three-dimensional structures. Finally, circuits and apparatus according to the invention can be literally, physically flexible when made in a wide range of embodiments.

A major aspect of the present invention is that it provides opportunities for creating integrated circuits of a radically new type, where electronic and/or optical functionality is embedded throughout the woven, knitted, crocheted, knotted and/or stitched structures, with the strands in the structures acting as signal and power conduits and creating or promoting structural integrity. As shall be described in detailed examples below, the strands can provide many forms of functionality, either at points where different strands come into physical contact with each other and create junctions that exhibit e.g. luminescence, memory or switching behaviour, or in restricted regions where strands are exposed to external influences such as light, heat or chemical species, or distributed along portions of the length of individual strands, or at specific points where attachment has been made to discrete functional components.

Figures 1, 2 and 3 give examples of standard weaving and knitting patterns and combinations thereof which are applicable, bur not exclusively, to generate circuits and devices which then form an electronic or opto-electronic fabric as used in the apparatus according to the present invention.

The fibers, wires, ribbons composing the circuits can have cross sections that are round, oval, square, rectangular, polygonal or any other desired shape as shown in fig. 4a. They may be single-component or multicomponent as shown in fig. 4b-d. For purpose of clarity these are all referred to as fibers in the following text. The components of multicomponent fibers can be arranged in different ways depending on the needs and applications. For instance a given fiber can be multicomponent in the crosssection and/or along the axis of the fiber, causing it to exhibit spatially varying physical, chemical and/or electrical properties. The single-component fibers and different components in multicomponent fibers may be either electrically conductive, semiconducting, superconductive, insulating, optically conductive or any combination thereof, but are not limited to these. The components can be any sensor or detector material such as those activated by light, heat, chemicals, electric and magnetic fields. Individual fibers, single component or multicomponent ca be bundled or braided as shown in fig. 4e.

The electronic or optoelectronic fabric can be composed of single component or multicomponent fibers combined in various ways as exemplified by the patterns in fig. 1, 2 and 3. The fabric can also be assembled from bundles or

braided fibers, or from more complex filament-like structures such as electrical cables with multiple conductors separated by a dielectric. Fibers of different types and different dimensions can be combined in the fabric. For example, alternating conducting and insulating fibers might be useful in some applications. The crossing of two or more fibers in the fabric are natural loci for device functionality such as memory, switches, sensors, etc. The crossing can be left as such or fused or bonded depending on the desired product.

There are no size limitations for these devices by the present invention. Individual devices can be created by weaving a given pattern at a chosen position in the fabric matrix as illustrated in fig. 5 for a loop detector and in fig. 6 for a pile sensor. The inclusion of a pile of small sensor fibers in the matrix will yield a high surface area detector, therefore high sensitivity. Such devices can be woven, knitted or stitched into the fabric matrix.

Such functional fabrics units and devices can be further combined by being woven or stitched or knitted into a larger fabric as illustrated in fig. 7. Multilayers knitting is also possible if necessary. The electronic fabric can be finally impregnated with any substance such as an insulator.

The circuit or optoelectronics thus fabricated can be addressed from the edges of the fabric or anywhere in the matrix by weaving, knitting or stitching in connecting wires.

Fig. 8a-c shows a display device or two-dimensional photodetector in matrix form as rendered in figs. 8a,c. It is assembled by weaving two types of fibers as shown in figs. 8a,b. One is a bi-component fiber with a core consisting of a conducting material M1 coated with an active material A which for this embodiment is either an electroluminescent material or a photoconductive material. The other fiber is a conductor M2. M1 and M2 will typically have different work functions. Each crossing then becomes a pixel of the two-dimensional array, as in fig. 8c. For a colour display panel, the electroluminescent material can be varied from one fiber to the next. For instance, three successive fibers will correspond to the three colours: red (R), green (G) and blue (B). Alternatively, different voltages can be used to generate different colors at each pixel. The pixel density achieved by the invention will be much higher than those of prior art. The high density of pixels in such a fabric is ideal for high definition applications.

Fig. 9a shows a memory or a switching array, where specific addresses in the array are located in a crosspoint matrix fashion, i.e. by selectively activating the row and column that cross at the point where the memory or switching cell is located. Variants of this basic scheme are employed extensively in the electronics industry, often with semiconductor components embedded within the matrix structure.

Typical embodiments of crosspoint matrices within the present state of the art are built on a silicon chip, where traditional lithographic silicon technologies are used to create the conducting matrix gridlines, etc. According to the present invention, however, the rows and columns in a matrix addressing system can be formed by wires crossing each other in a weave. An example is given below.

A class of memory devices that are of particular interest in conjunction with novel thin film and organic electronic materials employ passive matrices, i.e. matrices where the functional cell at each crossing point is very simple, without intra-cell transistor-based switching circuitry. One way of achieving addressability is to employ rectifying diodes to block parasitic current paths between the two wires that cross at the selected cell, cf. fig. 9b. Such "sneak currents" are a well-known problem in passively addressed matrices, as is the remedy of inserting diodes at the crossing points. Unfortunately, achieving this by traditional semiconductor techniques (lithography, etching, doping, plating...) is complicated and gives no competitive advantage over the alternatives, which are the well-known active-matrix based architectures used in ROMs, DRAMs, SRAMs, etc.

Recently, it has been shown, for instance in the International Patent Application PCT/NO98/00185 which has been assigned to the present applicant, that very compact and simple matrices with diode-connected crossing points can be made by using conjugated polymers that spontaneously create a diode junction when the polymer contacts a metal surface. This opens up opportunities for passive matrix memory devices where high-functionality organic and/or inorganic materials fill the volume between the crossing matrix electrodes, performing memory and addressability functions. A generic cell is shown in fig. 9c. Here, one of the electrodes is contacting a material which forms a rectifying junction at the electrode/material interface, while the rest of the cell volume is filled with a

memory material which controls the electrical characteristics of the cell according to the logic state (e.g. storing a logic "0" or "1"). This memory material may simply be a masked insulator in the ROM case, or it may be a material which can be switched between a high and a low impedance state to form a WORM (Write Once Read Many times) or ERASABLE (write, erase, write...) memory cell. Variants of the cell in fig. 9c include cells with only a single material which simultaneously takes care of the memory and addressability (e.g.: rectifying) functions.

In the prior art as illustrated in fig. 9c, the cells are formed by sandwiching the material in the cell (i.e. the memory and addressability layers) between a set of bottom electrodes that are typically pre-formed on a planar substrate, and a set of top electrodes, which are typically deposited onto the material in the cell and patterned by additive or subtractive processes. The simplest and most compact solutions are obtained when the materials in the cell are part of a layer that is applied globally, without patterning. This, however, implies certain drawbacks relating to restrictions on materials that can be used, as well as the ultimate cell density achievable (lateral leak currents in the cell materials).

In fig. 9d shows how a memory matrix with architecture equivalent to the one shown in fig. 9c can be made with crossing wires that are woven such that a memory cell is formed spontaneously at each point where wires in the weave cross. In the example shown, one set of wires extend in the x direction, the other set in the y direction. Each x wire consists of a monofilament metal, cladded by a polymer which forms a rectifying junction at the metal/polymer interface. Analogously, each y wire consists of a monofilament metal cladded by a substance which exhibits memory properties. An intimate electrical connection is formed between the cladding materials at the crossing point by mechanical force on the wires (pressure or stretching) during or after the weaving operation, assisted by thermal or chemical means. The basic structure in fig. 9c can be refined in different ways, e.g. by inserting electrically insulating separation filaments between the x and y wires in the matrix. Advantages of this woven approach are several as it provides a simple, virtually infinitely scalable means of creating passively addressed memory and switching matrices. Since the electrodes, memory and addressability materials are initially assembled as physically separated modules, one largely avoids chemical incompatibility problems which in

alternative schemes severely restrict the freedom of choice in materials and architectures.

With present invention a reduction of electrical interference and related noise mechanisms shall be possible by using dual- or multiple-conductor structures as threads in the joining process.

In devices the size of present day chips and with the same wire density and operating frequencies, the fabric-like architecture shall generally be much more favourable with regards to electrical interference immunity since the wires will be separated by air which minimizes the problem (low dielectric constant). See B. Shieh & al. "Air gaps lower k of interconnect dielectrics", Solid State Technology, pp. 51-58 (February 1999). In other large devices such as displays which operate at relatively low frequencies. the woven architecture will also be favourable over existing technology.

However, devices that employ a very dense weave with mutually parallel or crossing filaments carrying signal currents at high frequencies and/or over large areas are also of particular interest in the present invention. Important examples are device architectures where memory cells, logic circuitry, amplifiers and interfacing electronics are integrated in self-contained configurations on a common substrate. Clearly, crosstalk shall be a major problem if the interconnects are laid out in close proximity to each other on the substrate without very careful attention to capacitive and inductive pickup elimination. Several of the most potent strategies in this regard are difficult or impossible to implement when traditional manufacturing technologies are used, e.g. a planar substrate with etched or deposited conducting stripes, typically in adjacent planar layers mutually separated by insulating layers.

Weaving, knitting, crocheting, knotting and/or stitching techniques provide a unique opportunity to create devices where one needs to suppress cross-talk involving conductors that carry currents within and to/from the apparatus, as well as achieving controlled signal transmission properties in those conductors. Key to this is to employ two- or multiple-conductor transmission lines with closely controlled geometries that provide balanced current paths and shielding of electromagnetic fields. Such ultra-thin transmission lines could be manufactured before being incorporated as filaments in the weave.

Examples of such structures are twisted wire pairs, coaxial and certain types of stripline conductors as discussed in more detail in the following.

Using transmission lines with well-controlled electrical properties shall of course also present opportunities in addition to crosstalk suppression. An example is control of reflection properties at the terminations, of interest in high-speed circuits. Specific examples of types of transmission lines that can be embodied in the apparatus according to the invention are given below.

Example 1: Twisted pair filament conductors

See fig. 10a. The properties are well-known and extensively described in the electronic literature. Good immunity against inductive pick-up from magnetic fields. See, e.g.: P.Horowitz and W. Hill: "The art of electronics", pp. 456 et seq., Cambridge University Press, ISBN 0-521-37095-7. Each twisted pair of conductors could be used as one of the threads in the weaving process. This thread would then be a monolithic structure, with the conductor pair maintained in the desired positions relative to each other by a rigid dielectric matrix material.

Example 2: Coaxial line conductors

See fig. 10b. Each coax line, with inner and outer conductors as well as dielectric filling and coating materials, would constitute one of the threads in the weaving process.

In general, for a lossless coaxial line having the radii $r_a$ and $r_b$ for the outside radius of the inner conductor and inside radius of the outer conductor, respectively, one has the following parameters.

Capacitance per unit length (F/m): $C = 2\pi\varepsilon / \ln(r_b / r_a)$ (1)

Inductance per unit length (H/m): $L = (\mu/2\pi) \ln(r_b / r_a)$ (2)

Characteristic impedance ($\Omega$): $Zo = (\mu/\varepsilon)^{1/2} \ln(r_b / r_a) / 2\pi$ (3)

Propagation constant (m/s): $U = (\mu\varepsilon)^{-1/2}$ (4)

Here, μ and ε are the dielectric constant (electric permittivity) and magnetic permeability, respectively, of the fill material inside the coaxial line.

A major issue is that the transmission lines must retain the electrical properties of interest even as they are scaled down in size to ultra-thin outer diameters. In that connection, one may note from the expressions above that for lossless lines the characteristic impedances and propagation constants remain unchanged under linear scaling of the physical dimensions. This naive approach is generally corroborated by more realistic and thorough studies, under certain assumptions:

- Thus, the small cross-sections of the center and outer conductors imply that current paths must be short (typically a few centimeters), in order to keep resistive impedance low. This should present no problems in the present context.

- Furthermore, the thin outer conductor provides poor shielding of low frequency signals, highlighting the need for avoiding open loops by precisely controlled symmetric conductor geometries and uniform material properties in the line. The advantages in this connection of pre-forming the coax line before incorporating it into the substrate by weaving, instead of making such structures in situ are self-evident.

- Balanced current flows in the inner and outer conductors.

- Operate at moderate to high frequencies (MHz to GHz).

Example 3: Flat conductor pair

See figs. 10c-e, where 10c shows a planar line, 10d a strip line and 10e a symmetric strip line. Such transmission lines are high frequency signal compatible and well-known in the literature, cf., e.g.: P.Horowitz and W. Hill: "The Art of electronics", op. cit.

Example 4: Transmission lines in rolled-up devices

Novel devices of the generic type shown in fig. 11 shall now be discussed. Thin-film-based electronic and/or optoelectronic circuitry and components can as shown in fig. 11a be laid out on thin, flexible substrates which may in principle be of any shape or size. Thus, the size of the memory in data storage devices can be scaled by employing a substrate of appropriate size. Very large area substrates in the form of thin, flexible foils must be packaged

into practical form factors. This can be achieved by stacking, folding or rolling (fig. 11b) together the thin device-bearing substrates, whereby also high volumetric densities ensue. A recurring problem with such schemes is how to provide electrical connections to all parts of the large areas involved. Thus, when thin sheets are stacked on top of each other, connecting wiring to each sheet or between sheets in a stack may represent an unacceptable cost or reduce technical performance.

The rolled-up scheme in fig. 11b is attractive in that signal and power access can be established for a large-area, continuous structure, with only a few external connections entering the reel at the end of the rolled substrate. However, this solution implies that signal and power lines may become very long, extending along the full length of the rolled substrate. If traditional lithographic or printing technologies are employed to create these signal and power lines, signal attenuation along the length of the roll, reflections at signal branching and tapping points, and crosstalk between lines shall have a negative impact on technical performance, especially for high speed applications. Also, the creation of very long conducting lines by lithography or printing implies vulnerability to defects at points along the conductor. Instead, the present invention teaches the use of transmission lines in the form of multicomponent, balanced structures, i.e. micro-cables or -wires that can be manufactured to consistent high quality in a separate production step prior to being incorporated into the rolled sheet. The latter can be done in several ways, e.g.:

- The transmission line can be stitched into a ribbon that provides a uniform sheet-like substrate made from e.g. a polymer.

- The transmission line can constitute one of the strands in a woven ribbon-like substrate which forms the rolled-up device.

- A woven or braided length of multistranded material can be glued or laminated onto a ribbon of flexible sheet substrate.

*

Since the transmission lines have well-defined characteristics, precise impedance matching can be used to tap the lines at separate points along the length of the rolled-up sheet without corrupting the signals.

The power and signal lines may be optical as well as electrical. In the optical case, printing and lithography techniques are even less competitive as compared to the use of fibers or cables. even over short propagation distances: Although optical waveguides deposited or etched on planar substrates are well-known, e.g. as optical circuit elements, typical propagation distances are of the order of centimeters. Optical fibers, on the other hand, are widely used in signal transmission over thousands of kilometers.

The filament diameters of relevance in woven electronics applications shall typically be small, i.e. < 100 microns. There exists a large body of knowledge within the general field of joining processes, etc, derived from the textile industry, and this encompasses technologies for handling ultra-thin filaments. In the present context, however, certain new elements are introduced, i.e. the requirement that at least some of the individual filaments shall possess explicit electrical and optical transmission properties. This shall not necessarily imply any major departure from traditional weaving technologies as long as monofilaments of metals or optical glasses or plastics are concerned. However, dual- or multiple-conductor filaments represent a novel aspect, both as regards the manufacture of the conductor structures themselves and their incorporation into woven devices.

Coaxial lines are of particular interest in the present context. Micro-coaxial cables are extensively used in low power level, high frequency applications, e.g. radar signal conditioning. To our knowledge, the thinnest commercially available cables are approximately 0.5 mm. in outer diameter, i.e. too coarse for fabric-like or woven electronics applications. On the other hand, there is no principal reason why much thinner coaxial cables could not be made. Indeed, there is presently being conducted research on nanoscaled electronic devices which also includes ultraminiature electrically conducting wires and sheathed cable, cf.: Y. Zhang et al.: "Coaxial nanocable: Silicon Carbide and Silicon Oxide Sheathed with Boron Nitride and Carbon", Science, Vol.281, pp. 973-975 (August 14, 1998).

Below the connection to specific conductors at selected locations inside the weave shall be considered in more detail.

In the fabric-like or woven electronics concept, there is a need to couple selected conductors in the weave electrically to components and other

conductors, at well-defined points in the weave. This task is non-trivial in cases with a highly dense weave consisting of ultra-thin, possibly coated conductors running all the way from the edge of the weave. Some basic principles that can be followed:

- Insert locally a wire which is just stripped at the tip to make electrical contact while the rest of the wire is coated with an insulator. The inserting of fibers or filaments locally is a common fabric technology.

- Insert an optical fiber or fiber bundle to send signals to and from a photodetector/emitter.

- Post-insertion stripping or other treatment of localized areas on fibers, wires and filaments to gain access to the signal or power paths can be performed in a number of ways. For example, using openings in a patterned mask lithographically defined directly on the weave or through a membrane in proximity, selected portions of the electrically insulating material surrounding conducting wires can be removed by etching or they can be modified by doping.

Alternatively, one may employ a beam which writes the positions where conductors are to be exposed, either by direct erosion (ion beam) or indirectly via a sensitizing beam.

In many cases, it is useful to separate conducting leads in the weave from each other by inserting intermediate insulating strands in the web. This simplifies the task of avoiding unintentional stripping of the coating layer on conductors close to the one to be connected. Another way of avoiding contact with near-lying strands is to employ coated conductors with different dissolution properties for the coatings, cf. the specific following examples.

Example 5

In a line of the "twisted pair" type consisting of two metal filaments with insulated coatings applied on each separately before being twisted together: There are two types of coating, one for the "hot", one for the "cold" filament, where the solubilities of the coatings in specific chemicals are different. The metal core in the "hot" filament would then be laid bare at a given location by selectively dissolving the coating on that filament using a chemical etchant which only attacks the "hot" filament coating.. The extent of the

dissolution region could be controlled by exposure to the chemical etchant through a lithographically defined opening in a protective film.

Example 6

A variant of Example 1 is localized selective sensitization followed by chemical etching: The "hot" filament coating would be made soluble to a given reagent in desired locations, by exposure to the sensitizing agent (vapor, liquid, light, heat, particle beam....) through a lithographically defined opening in a protective film.

Example 7

The same basic principles as in Examples 5 and 6 can be employed with other types of selective stripping methods than chemical dissolution. Such methods include dry etching by photon (e.g. eximer laser) or particle irradiation, exploiting differences in etching rates of the coatings. The latter may be linked to, e.g. different hardness of the coating materials or to differences with respect to absorption of the irradiating photons or particles, or differences in etching rates

Example 8

Instead of using lithography to define the areas that shall be subjected to etching, one may use inkjet printing to either deposit the protective layer or the etching agent itself.

Example 9

Instead of using lithography to define the areas that shall be subjected to etching, one may use vector or raster scanning of a light or particle beam to achieve localized etching or sensitization. This way, several production steps can be avoided.

The advantages of the present invention are several. Electronic and optoelectronic functionality can be achieved on a wide scale of complexity and degree of integration in scalable two- or three-dimensional structures that are physically robust and flexible with respect to form factor. Integration of both optical and electronic circuits is simplified since material compatibility is not an important issue. Yet another advantage of the invention is the flexibility in the circuit design which can be continuously changed and adapted to meet specific needs. Wires can be looped and structured in such a way as create functional devices at any point or area in the woven matrices.

The invention also provides a simple way to produce defect-tolerant architecture. See Heath & al., op. cit.

With the present invention a whole new class of electronics and/or optoelectronic apparatus will be possible. Particularly the invention offers the possibility of initially large-area flat devices which may be made as flexible fabric-like or woven structures and thus easily be form-adapted for specific purposes, in addition to being area-scalable. Such devices shall be well-suited for creating novel display devices and may as desired be made to be integrated with active and/or passive known electronic, optoelectronic or optical devices.

PATENT CLAIMS

1. An apparatus comprising electronic and/or optoelectronic circuitry for implementing electronic and/or optical functions, wherein the circuitry is realized and/or integrated in two or more dimensions, characterized in that the circuitry comprises elements in the form of wires, fibres, ribbons, strips, or multicomponent filaments and/or combinations thereof, said elements interfacing in a predetermined pattern such that said circuitry are realized with intersections in physical or near physical contact between the elements thereof, that said predetermined pattern is generated by integrating physically two or more of said elements in a fabric-like structure by any of the following processes, viz. weaving, knitting, crocheting, knotting, stitching and/or combinations thereof, that said elements include transparent, non-transparent, conducting, semiconducting or isolating materials and/or combinations thereof, that at least some of said elements according to their material properties form electrical or optical transmission lines or isolators in said circuitry, said electrical or optical transmission lines conveying respectively electrical or optical energy between points and/or areas in said fabric-like structure, that at least some of said elements comprise spatially defined extended active regions, and that at least some of said elements in portions of said fabric-like structure are adapted for emitting or absorbing electrical, chemical, mechanical or optical energy or by interacting with each other by an exchange of energy of the aforementioned kinds.

2. An apparatus according to claim 1, characterized in that the elements are provided in the predetermined pattern forming a substantially two-dimensional fabric-like structure.

3. An apparatus according to claim 1, characterized in that the elements are provided in the predetermined pattern forming a substantially three-dimensional fabric-like structure.

4. An apparatus according to claim 3, characterized in that the elements each has a length and are provided in a spatial distribution such that the positions of the end-points of the elements in the fabric-like structure define a spatial pattern or grid.

5. An apparatus according to claim 1, characterized in that some of the transmission lines are twisted pairs.

6. An apparatus according to claim 1, characterized in that some of the transmission lines are coaxial cables.

7. An apparatus according to claim 1, characterized in that some of the transmission lines are striplines.

8. An apparatus according to claim 1, characterized in that some of the transmission lines are optical fibres.

9. An apparatus according to claim 1, characterized in that the active regions of the elements are defined by exposing portions of the elements to the exterior surroundings thereof.

10. An apparatus according to claim 1, characterized in that active regions of an element are lengthwise extended therein.

11. An apparatus according to claim 1, characterized in that an active region of an element corresponds to an end-point thereof.

12. An apparatus according to claim 1, characterized in that some of the elements are provided with a protective shielding or cladding, the active regions in these elements being provided by removing the shielding or cladding at selected portions thereof.

13. An apparatus according to claim 1, characterized in that the active regions of the elements are provided in selected portions of the elements exposed in the surface of the fabric-like structure or protruding therefrom at selected locations thereof.

14. An apparatus according to claim 1, characterized in that the active regions of the elements are defined by exposing portions thereof to spatially selective physical or chemical influences.

15. An apparatus according to claim 14, characterized in that some of the transmission lines are at least one conductor embedded in an exterior cladding comprising at least one organic semiconducting material, and that active regions are defined therein by contacting said transmission lines with other transmission lines of the same kind or with other transmission lines in intersections which comprise at least one non-isolated or unclad conductor

only, whereby semiconducting junctions are formed at the contact points of said intersections.

16. An apparatus according to claim 15, characterized in that the semiconducting junctions are formed spontaneously upon contacting.

17. An apparatus according to claim 15, characterized in that at least one of the semiconducting junctions are a diode junction.

18. An apparatus according to claim 15, characterized in that the organic semiconducting material is a semiconducting conjugated or non-conjugated polymer.

19. An apparatus according to claim 1, characterized in that at least some of the elements over some of their length are shielded against any interactions in form of an exchange of energy between each other or the exterior surroundings, whereas one or more unshielded portions thereof are adapted for interactions of this kind.

20. An apparatus according to claim 19, characterized in that the unshielded portions of the elements are located at the intersections thereof.

21. An apparatus according to claim 1, characterized in that an apparatus is a two- or three-dimensional optoelectronic display.

22. An apparatus according to claim 21, characterized in that the elements are signal transmission lines.

23. An apparatus according to claim 21, wherein the display is a two-dimensional display, characterized in that the elements are provided in a two-dimensional array.

24. An apparatus according to claim 23, characterized in that the elements intersect in a substantially regular pattern or grid, said elements at the intersections thereof being adapted for absorbing or emitting electrical or optical energy.

25. An apparatus according to claim 24, characterized in that a portion of at least one element in an intersection is a pixel of the display.

26. An apparatus according to claim 21, wherein the display is a three-dimensional display, characterized in that the elements are provided in a three-dimensional array.

27. An apparatus according to claim 26, characterized in that the elements intersect in a spatial regular pattern or grid, said elements in intersections thereof being adapted for emitting or absorbing electrical or optical energy.

28. An apparatus according to claim 26, characterized in that a portion of at least one element in an intersection is a pixel of the display.

29. An apparatus according to claim 26, wherein active regions of the elements are provided in selected portions of the element exposed in the surface of the fabric-like structure or protruding therefrom at selected locations thereof, characterized in that active regions of this kind are pixels in the display, said active regions being either a loop-like portion of an element or an end-point thereof.

30. An apparatus according to claim 1, characterized in that an apparatus comprises respectively one or more discrete electronic, optoelectronic or optical devices or combinations thereof.

31. An apparatus according to claim 30, characterized in that one or more of the discrete devices are physical or chemical sensors connected to at least one of the elements.

32. An apparatus according to claim 1, characterized in that one or more of the elements are a physical or chemical sensor.

33. A method for realizing and/or integrating circuitry in two- or more dimensions, wherein the circuitry comprises elements in the form of wires, fibres, ribbons, strips or multicomponent filaments and/or combinations thereof, wherein said circuitry is electronic and/or optoelectronic circuitry for implementing electronic and/or optical functions in an apparatus comprising circuitry of this kind, characterized by joining two or more elements into a fabric-like structure by any of the following processes viz. weaving, knitting, crocheting, knotting, stitching and/or combinations thereof, such that the elements interface in a predetermined pattern, whereby the circuitry is realized with the elements intersecting in physical or near-physical contact in the fabric-like structure, said elements being made of transparent.

non-transparent conducting, semiconducting or isolating materials and/or combinations thereof.

34. A method according to claim 33, characterized by providing the surface of the elements with a shielding or cladding material before joining into the fabric-like structure, and by removing said shielding or cladding material after the joining into the fabric-like structure from some elements or from selected portions thereof at selected locations in the fabric-like structure.

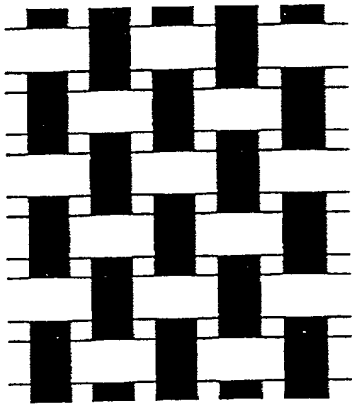

Fig.1a

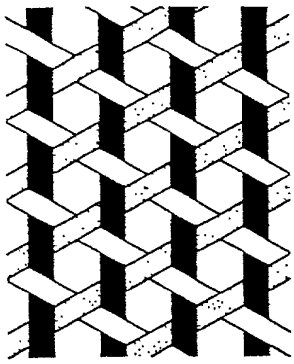

Fig.1b

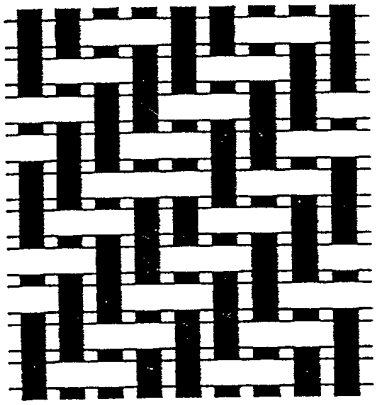

Fig.1c

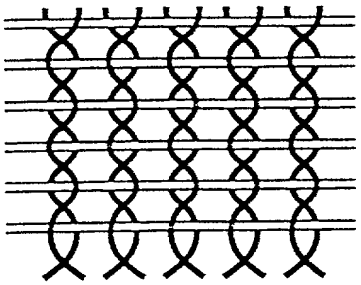

Fig.1d

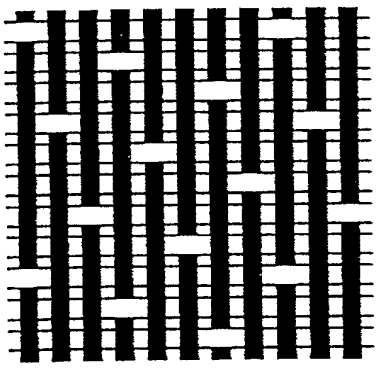

Fig.1e

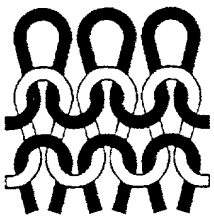

Fig.2a

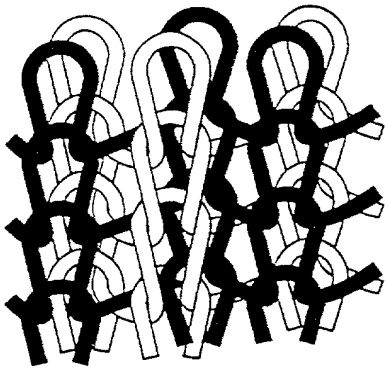

Fig.2b

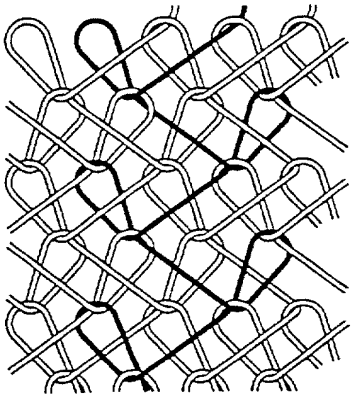

Fig.2c

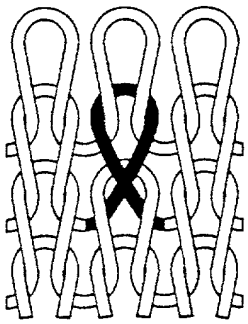

Fig.2d

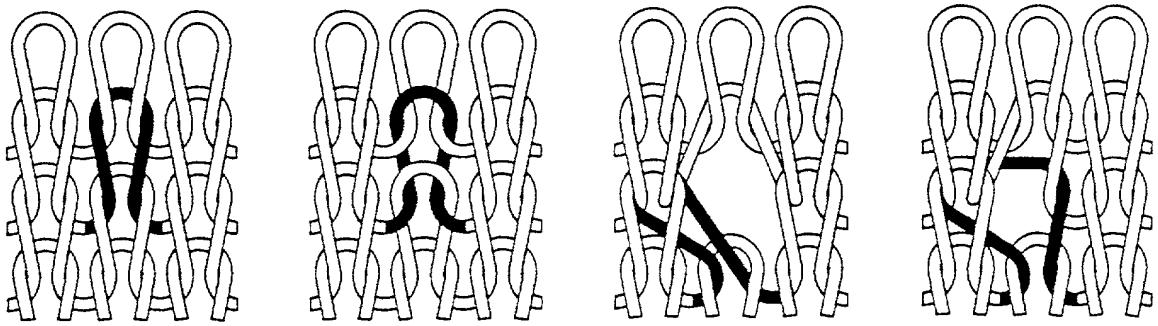

Fig.2e

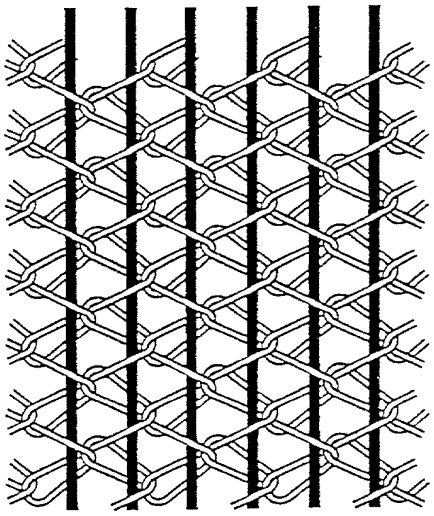

Fig.3a

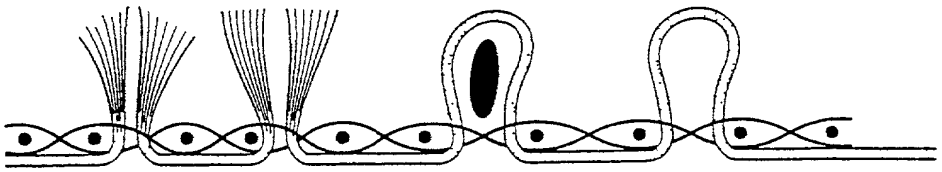

Fig.3b

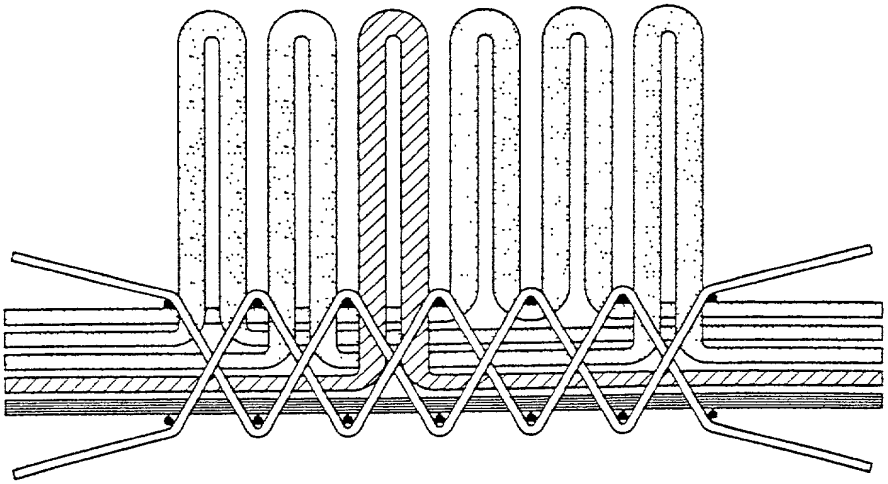

Fig.3c

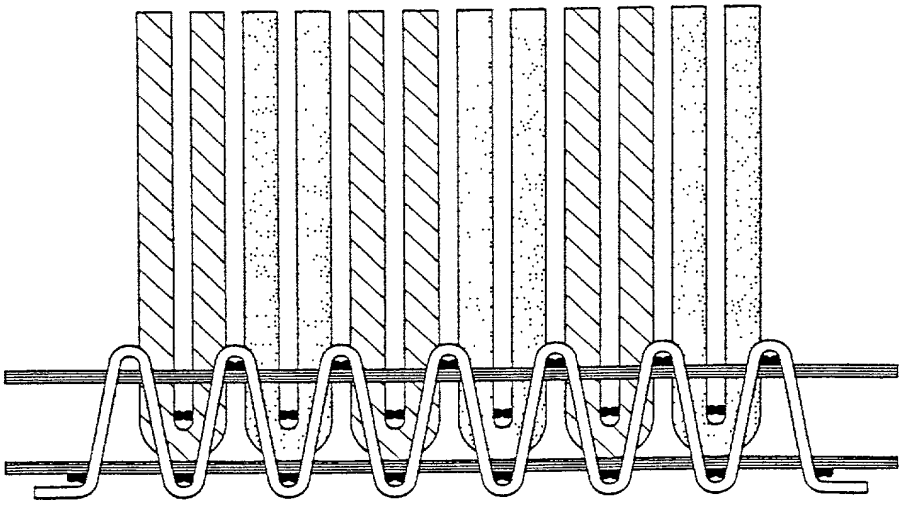

Fig.3d

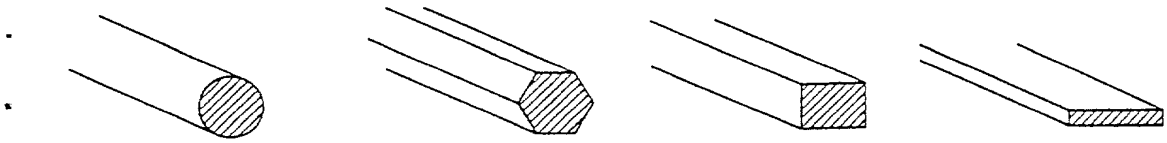

Fig.4a

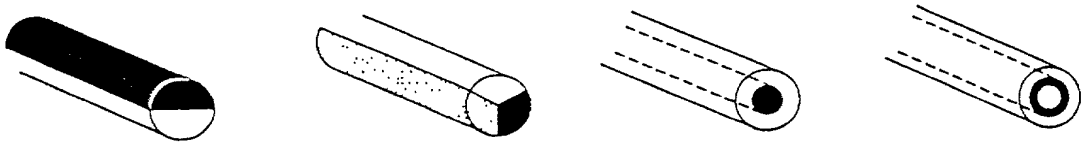

Fig.4b

Fig.4c

Fig.4d

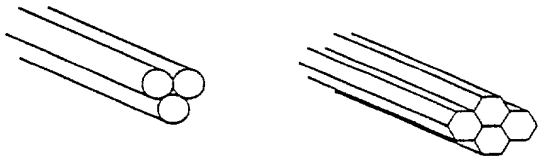

Fig.4e

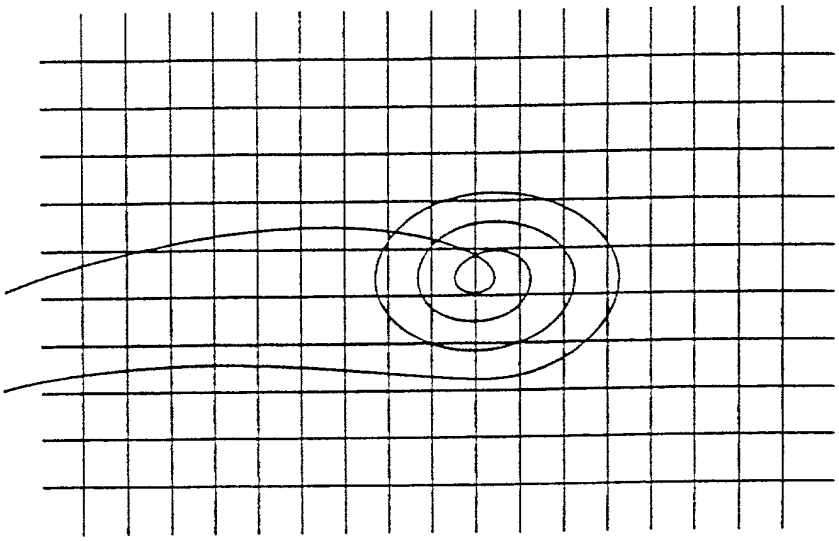

Fig.5

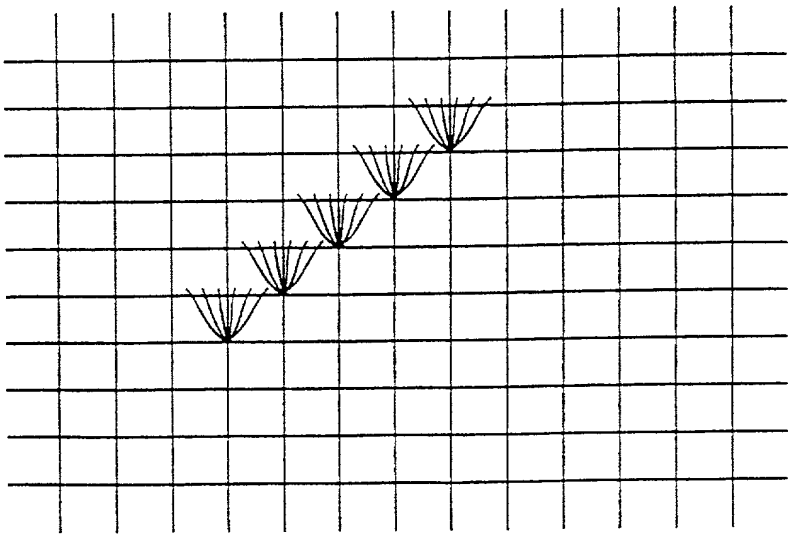

Fig.6

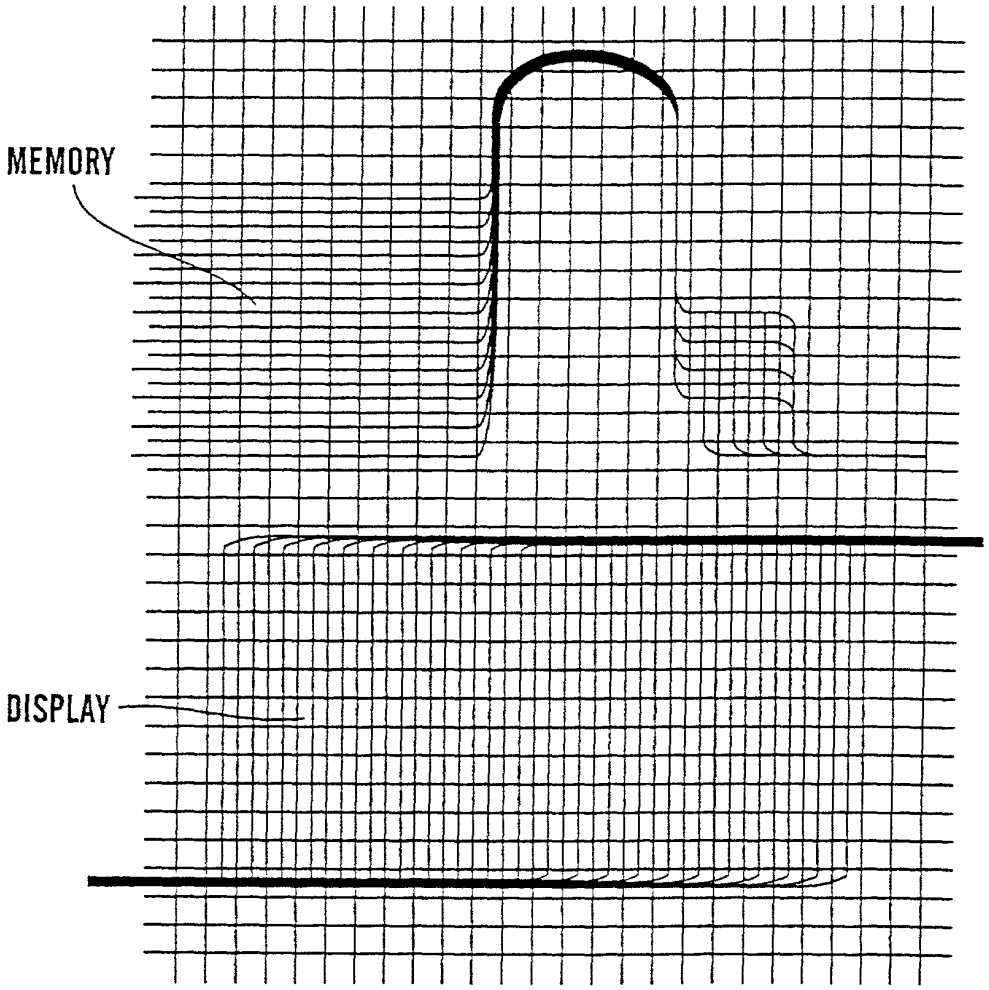


Fig.7

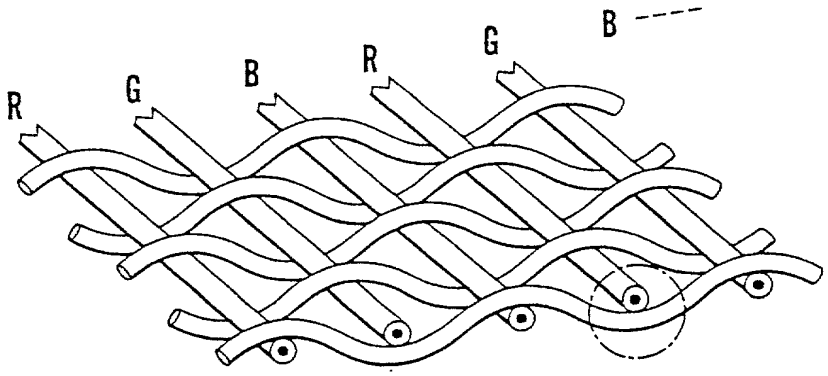


Fig.8a

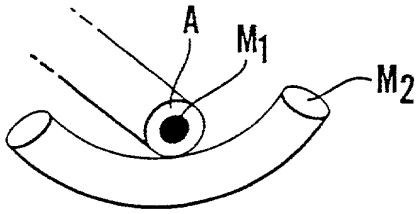


Fig.8b

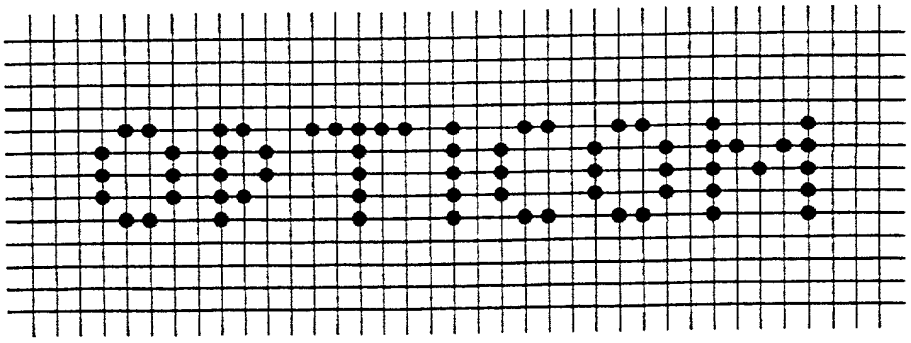

Fig.8c

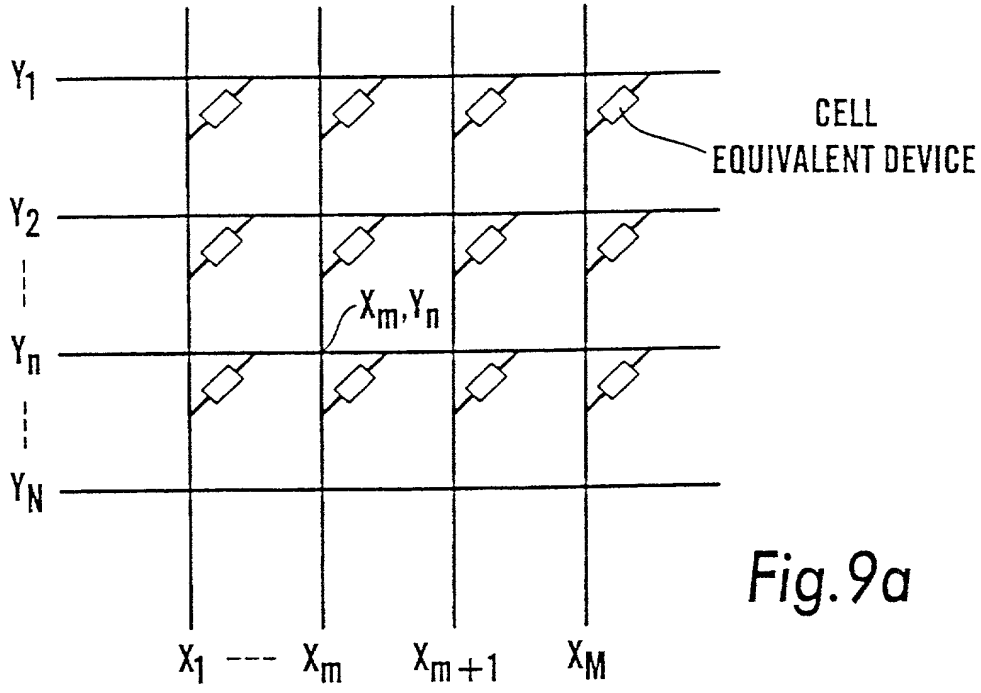
Y1
Y2
Yn
YN
Xm,Yn
CELL
EQUIVALENT DEVICE
X1 --- Xm Xm+1 XM

Fig.9a

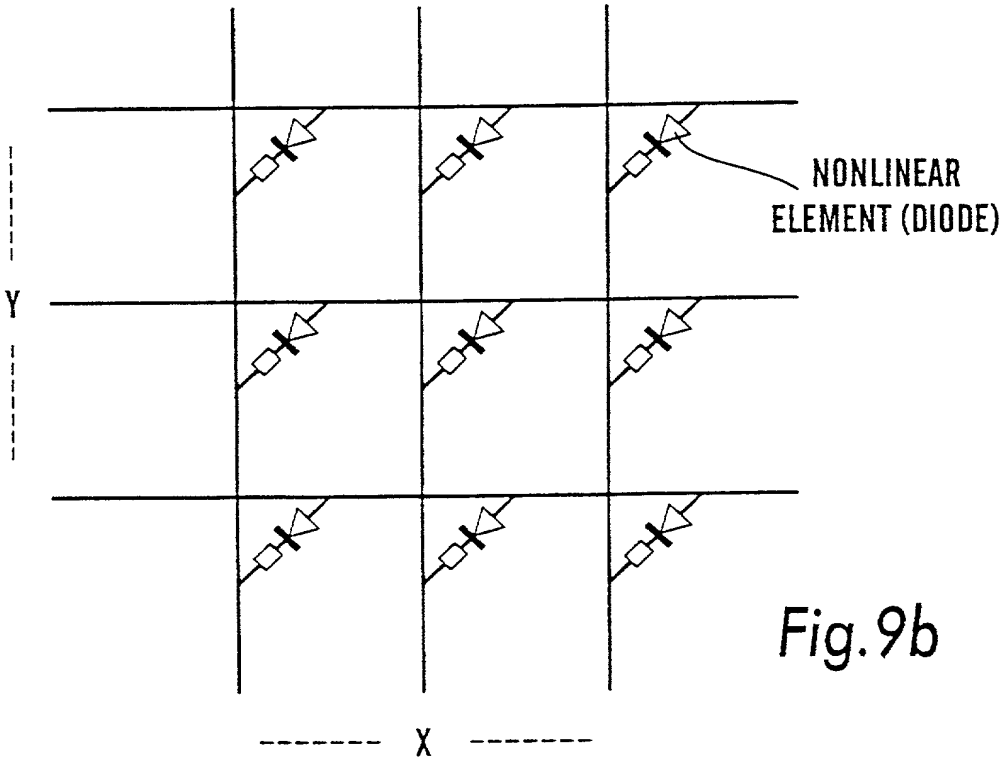
NONLINEAR
ELEMENT (DIODE)
Y
X

Fig.9b

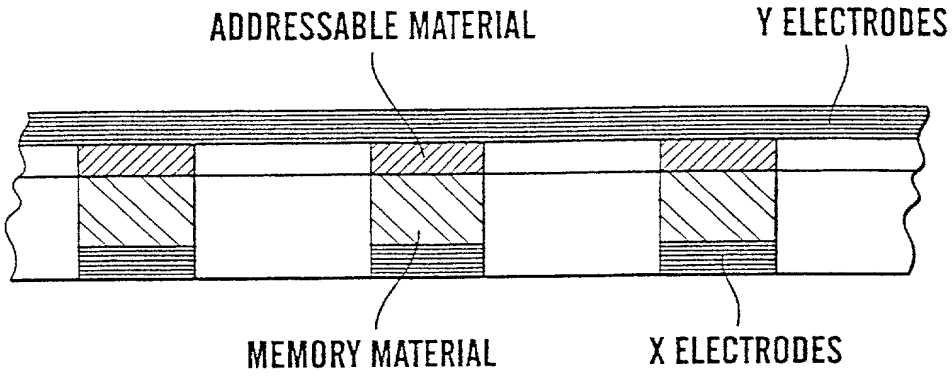
ADDRESSABLE MATERIAL
Y ELECTRODES
MEMORY MATERIAL
X ELECTRODES

Fig.9c

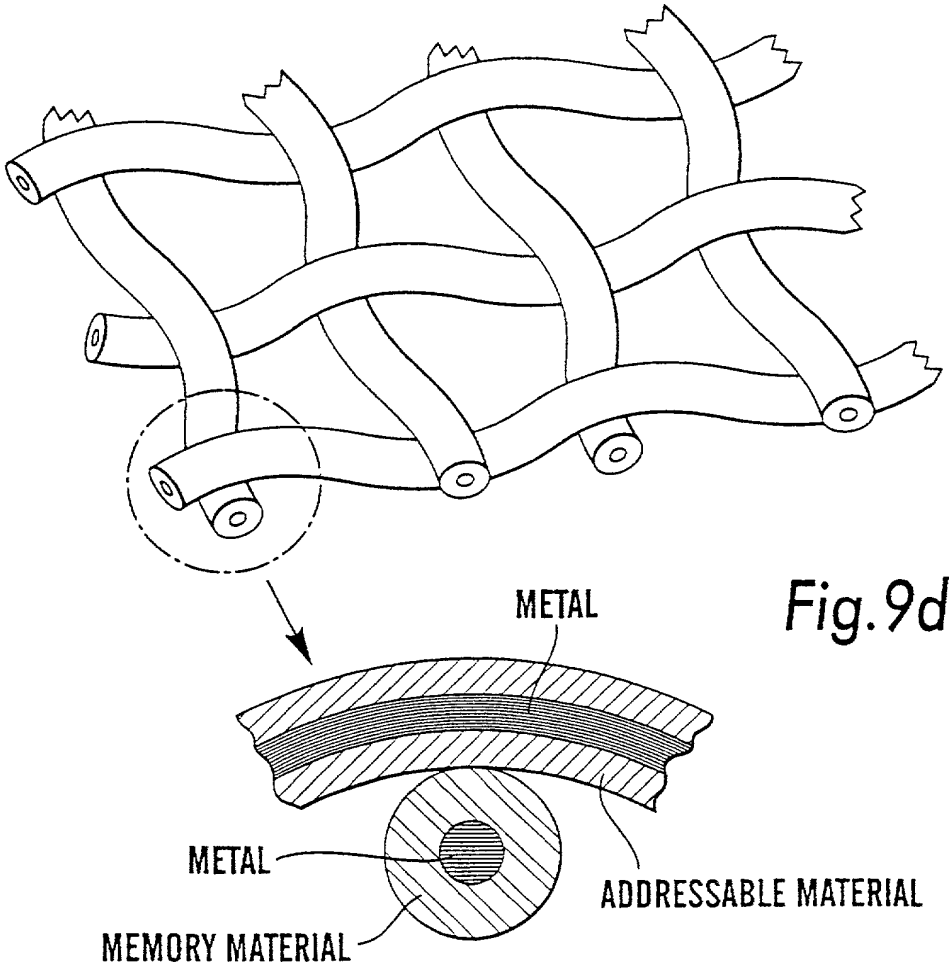
METAL
METAL
ADDRESSABLE MATERIAL
MEMORY MATERIAL

Fig.9d

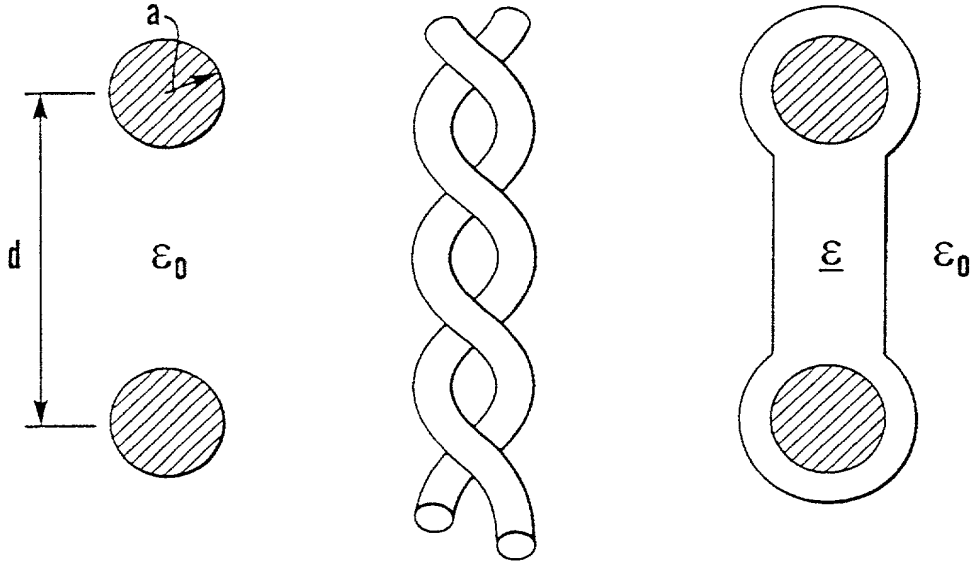


Fig.10a

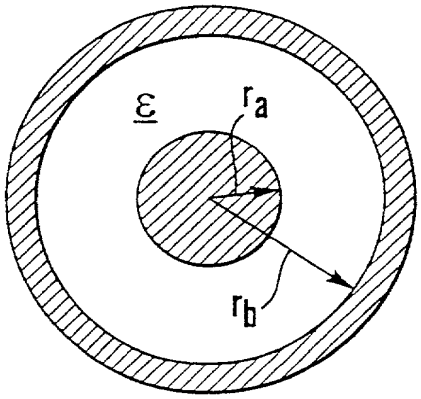


Fig.10b

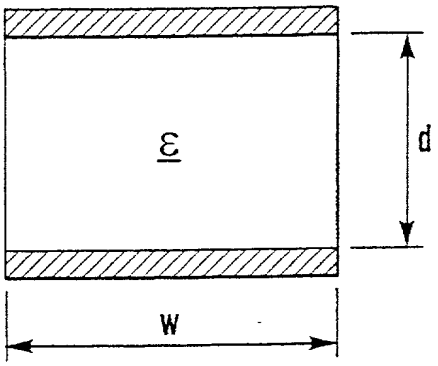


Fig. 10c

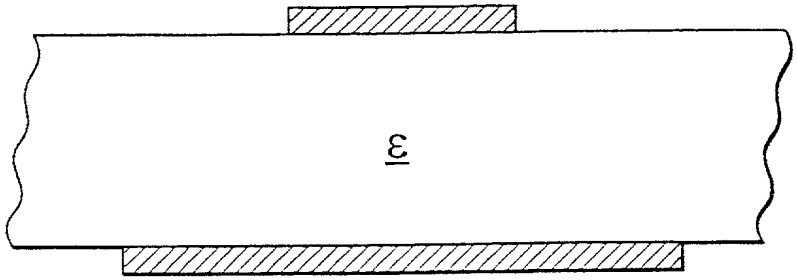


Fig. 10d

Fig. 10e

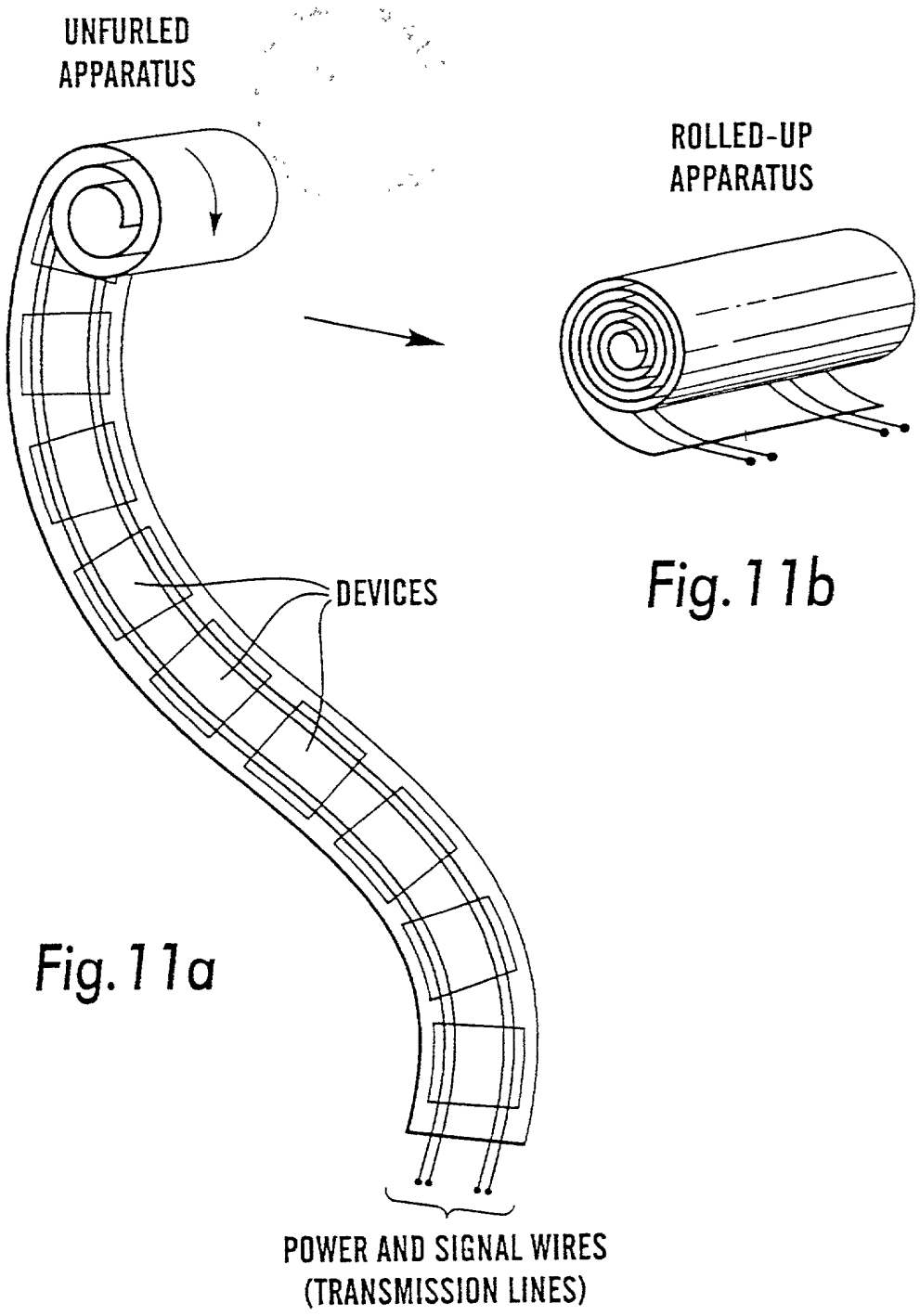


Fig.11b

Fig.11a

# BIRCH, STEWART, KOLASCH & BIRCH, LLP

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

## COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO. 3672-0109P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor ( if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**Insert Title:** ➡ An apparatus comprising electronic and/or optoelectronic circuitry and method for realizing said circuitry

**Fill in Appropriate Information - For Use Without Specification Attached:** ➡

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____; and /or

the specification was filed on 27 April 2000 as PCT
International Application Number PCT/NO00/00137; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

**Insert Priority Information: (if appropriate)** ➡

| Prior Foreign Application(s) | | | Priority Claimed | |
|---|---|---|---|---|
| 19992124 (Number) | Norway (Country) | April 30 1999 (Month/Day/Year Filed) | ☒ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |
| (Number) | (Country) | (Month/Day/Year Filed) | ☐ Yes | ☐ No |

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

**Insert Provisional Application(s): (if any)** ➡

(Application Number) (Filing Date)

(Application Number) (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

**Insert Requested Information: (if appropriate)** ➡

| Country | Application No. | Date of Filing (Month/Day/Year) |
|---|---|---|
| | | |
| | | |

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

**Insert Prior U.S. Application(s): (if any)** ➡

| (Application Number) | (Filing Date) | (Status - patented, pending, abandoned) |
|---|---|---|
| | | |
| | | |

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

| | | | |
|---|---|---|---|
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| Joseph A. Kolasch | (Reg. No. 22,463) | James M. Slattery | (Reg. No. 28,380) |
| Bernard L. Sweeney | (Reg. No. 24,448) | Michael K. Mutter | (Reg. No. 29,680) |
| Charles Gorenstein | (Reg. No. 29,271) | Gerald M. Murphy, Jr. | (Reg. No. 28,977) |
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**PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**Full Name of First or Sole Inventor:**
**Insert Name of Inventor**
**Insert Date Thus Document is Signed**

| GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE* |
|---|---|---|---|
| Thomas | EBBESEN | | 9 November 2000 |

**Insert Residence**
**Insert Citizenship**

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see above

| GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE* |
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**Full Name of Third Inventor, if any**

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| GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE* |
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|---|---|
| | |

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**Full Name of Fourth Inventor, if any**

see above

| GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE* |
|---|---|---|---|
| | | | |

| Residence (City, State & Country) | CITIZENSHIP |
|---|---|
| | |

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

**Full Name of Fifth Inventor, if any**

see above

| GIVEN NAME | FAMILY NAME | INVENTOR'S SIGNATURE | DATE* |
|---|---|---|---|
| | | | |

| Residence (City, State & Country) | CITIZENSHIP |
|---|---|
| | |

POST OFFICE ADDRESS (Complete Street Address including City, State & Country)

* DATE OF SIGNATURE